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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,245	02/02/2004	Jean Y. Yang	H0698	9469

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RENNER, OTTO, BOISSELLE & SKLAR, LLP (AMDS)
1621 EUCLID AVE - 19TH FLOOR
CLEVELAND, OH 44115-2191

EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,245	YANG ET AL.	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the election filed 3/21/05.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-19 in the reply filed on 3/21/05 is acknowledged. The traversal is on the ground(s) that no reasons for traversal are given. This is not found persuasive because no reasons for traversal are given.

The requirement is still deemed proper and is therefore made FINAL.

2. Claim 20 is withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 3/21/05.

3. Applicant's election of claims 1-19 in the reply filed on 3/21/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

4. The drawings are non-compliant with 37 CFR 1.84(p)(3), which states that lettering and numbering in a patent drawing "must" measure minimum 1/8 inch height. The "As" in Fig. 1, for example, is too small for quality printing of a patent. Correction is required.

5. The "layer" comprising layers "324" and "322". in Fig. 13 is referred to as "dielectric layer 318" at p. 20, yet the drawings do not include a "318." The missing reference "318" should be added to Fig. 13 with a bracket around layers 322 and 324 (analogous to layer 18a bracketing layers 22, 24 and 26a in Fig. 6). Correction is required.

6. In Fig. 13, the reference numerals "422, 424 and 426'. designate "multiple layers" (p. 20, line 24) that form "dielectric layer 418," but the numerals "422 " "424 " and "426" do not appear in the specification. Correction is required.

Specification

7. The disclosure is objected to because of the following informalities: Page 2, line 23 recites "multiplayer". It is believed the applicant meant "multilayer"..

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 12 recites the limitation "the first dopant type is boron and the second dopant type is arsenic" in claim 11. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-12 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kamal (US006479348B1).

Kamal teaches all of the positive steps of claims 1-12 and 18 as follows.

Regarding claim 1, Kamal teaches a charge trapping layer over a substrate (504), forms a doped region in the substrate (threshold adjustment implant, step 604), forms buried bitlines in the doped region (512, step 608). Regarding the limitation that the doped region adjacent the at least one bitlines inhibits leakage current between the buried bitlines, this is functional language.

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be used does not differentiate the claimed apparatus from the prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App.& Inter. 1987) MPEP 2114.

Further, as the positive steps are identical, the same functional result would occur. Also, "inhibits" is a qualitative term. The doping of Kamal inhibits leakage as compared to a region without doping.

Regarding claim 2, the charge trapping layer contains multiple regions and functions for programming and erasing (column 3 lines 41-42).

Regarding claim 3, a conductive layer (515) is formed over the charge trapping layer which is itself between the conductive layer (515) and the substrate (501).

Regarding claim 4, the charge trapping layer is a multi-layer dielectric layer (506, 508, 510).

Regarding claim 5, the multi-layer dielectric layer includes a charge trapping layer (508).

Regarding claim 6, the multi-layer dielectric layer is an oxide-nitride-oxide (ONO) layer (column 4 lines 40-47 and column 5 lines 15-23).

Regarding claim 7, the charge trapping layer (404 or 504) includes a tunneling layer (406 or 506), a charge trapping dielectric layer (408 or 508), and an insulating layer (410 or 510), and the tunneling layer is disposed over the substrate, the charge trapping

dielectric layer is disposed over the tunneling layer, and the insulating layer is disposed over the charge trapping layer (figure 5).

Regarding claim 8, the tunneling layer is SiO2 (column 4 lines 43-44).

Regarding claim 9, the material of the charge trapping layer is one or more materials of a permittivity greater than SiO2 (3.9) (the material is Si_xN_y, the same as the instant specification and has a permittivity of 7.5).

Regarding claim 10, the material of the charge trapping layer is Si_xN_y (column 4 lines 44-45).

Regarding claim 11, a hard mask layer (516, step 612 is formed over the charge trapping layer, depositing a photoresist (step 614), the photoresist is patterned (photomask step 616), and the pattern transferred to the hard mask layer (column 5 lines 33-42 and column 6 lines 27-43).

Regarding claim 12, the first dopant type (in a P-type substrate is boron (column 4 lines 31-33) and the second type is arsenic (column 4 line 53).

Regarding claim 18, Kamal teaches this to be a MirrorBit Flash memory and as such wordline (515) acts as a control gate (column 2 lines 16-18).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal (US006479348B1).

Kamal teaches all of the positive steps of claims 13-15 as recited above in regard to claim 11, except for the implanting of the doped regions and bitlines formed through the apertures in the hard mask.

Regarding claim 13, Kamal is silent as to implanting through a hard mask. Kamal does teach depositing, patterning and etching hard masks (column 5 lines 35-41) and that the doped regions and bitlines do not take up (individually) the entire substrate. Thus is obvious that the doped regions and bitlines are formed by implanting through apertures in a hard mask.

Regarding claim 14, Kamal teaches forming an insulating layer (500) over the hard mask. Kamal does not state that the material is planarized, but figure 8 shows planar

surfaces on the gates, thus it was planarized. Figure 7 shows that prior to removal, the material filled the apertures of the hard mask.

Regarding claim 15, figure 6 shows removing (part of) the hard mask.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Kamal by implanting through apertures as it is obvious to implant into selected regions by implanting through apertures in a hard mask.

14. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal (US006479348B1) in view of Wolf (pages 298-299).

Kamal teaches all of the positive steps of claim 16 as recited above in regard to claim 11, except for annealing to repair damage after implanting. Kamal is silent as to annealing, but Wolf (pages 298-299) teaches that annealing must be performed to repair the damage caused by implanting.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Kamal by annealing as taught by Wolf to be necessary to repair damage after implanting.

15. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal (US006479348B1) in view of Yang (US005418176A).

Kamal teaches all of the positive steps of claim 17 as recited above in regard to claim 1, except for the charge trapping layer being conductive. Kamal teaches the layer to be insulative. Page 20 of the instant application teaches an alternate embodiment where the layer is conductive rather than insulating (as on pages 9-10), but teaches no criticality between the layer being conductive or insulative.
Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or of any unexpected results arising there from. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in the claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1515, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Yang teaches using a floating gate as a charge trapping layer, thus it is known to use a conductive layer for such a purpose.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Kamal by using a conductive layer as the charge trapping layer as taught by Yang to be known.

16. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal (US006479348B1) in view of Eitan (US005966603A).

Kamal teaches all of the positive steps of claim 19 as recited above in regard to claim 18, except for forming a multi-layer dielectric over the charge trapping layer and between the charge trapping layer and the control gate. Kamal teaches the layer to be a single layer. Eitan teaches the layer may be a single layer or a multi-layer (column 3 line 61-column 4 line 6), giving the two options an art recognized equivalence.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Kamal by using a multi-layer in place of the single layer as taught by Eitan to have an art recognized equivalence.

Information Disclosure Statement

17. The applicant is reminded that there is a duty to disclose information material to an application's patentability (37 U.S.C. 1.56). Also see MPEP 2001-2001.06(b).

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Google search permittivity, shows permittivity of silicon nitride to be higher than that of silicon oxide.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

May 25, 2005